WHAT IS CLAIMED IS:

1. A method for optimizing buffers in an integrated circuit design comprising:

identifying paths and nodes within the integrated circuit design;

determining node overlap within the integrated circuit design;

calculating possible solutions for addressing timing violations within the integrated circuit design;

choosing a solution for addressing timing violations;

inserting buffers at particular nodes of the integrated circuit design; and,

repeating the calculating possible solutions, the choosing a solution and the inserting buffers at particular nodes to address timing violations within the integrated circuit design.

2. The method for optimizing buffers in an integrated circuit design of claim 1 wherein

the repeating continues until a previous maximum number of violations have been addressed.

3. The method for optimizing buffers in an integrated circuit design of claim 2 wherein

after the repeating, there are orphan timing violations remaining to be addressed; and, further comprising

inserting buffers at particular locations to address the orphan timing violations.

4. The method for optimizing buffers in an integrated circuit design of claim 1 wherein

the choosing a solution is based upon fixing a plurality of timing violations based upon various input criteria.

5. The method for optimizing buffers in an integrated circuit design of claim 4 wherein

the various input criteria include a median approach, the median approach including calculating a nominal number of fixes from the calculating possible solutions and then selecting an approach which fixes more than the nominal number of fixes.

6. The method for optimizing buffers in an integrated circuit design of claim 4 wherein

the various input criteria include an acquisitive approach, the acquisitive approach including determining which solution from the calculating possible solutions fixes a greatest number of timing violations and then selecting the approach which fixes the greatest number of timing violations.

7. The method for optimizing buffers in an integrated circuit design of claim 1 further comprising:

identifying buffers from a list of potential buffers available to insert into the integrated circuit design; and

choosing a subset of the buffers from the list as buffers for inserting at the particular nodes of the integrated circuit.

8. The method for optimizing buffers in an integrated circuit design of claim 7 wherein:

factors used in choosing a subset of the buffers from the list as buffers include a first order delay characteristic of the buffer, a maximum time slack characteristic of the buffer, and a drive strength characteristic of the buffer.

9. A apparatus for optimizing buffers in an integrated circuit design comprising:

means for identifying paths and nodes within the integrated circuit design;

means for determining node overlap within the integrated circuit design;
means for calculating possible solutions for addressing timing violations within the integrated circuit design;
means for choosing a solution for addressing timing violations;
means for inserting buffers at particular nodes of the integrated circuit design; and,
means for repeating the calculating possible solutions, the choosing a solution and the inserting buffers at particular nodes to address timing violations within the integrated circuit design.

10. The apparatus for optimizing buffers in an integrated circuit design of claim 9 wherein
the repeating continues until a previous maximum number of violations have been addressed.

11. The apparatus for optimizing buffers in an integrated circuit design of claim 10 wherein
after the repeating, there are orphan timing violations remaining to be addressed; and, further comprising
means for inserting buffers at particular locations to address the orphan timing violations.

12. The apparatus for optimizing buffers in an integrated circuit design of claim 9 wherein
the choosing a solution is based upon fixing a plurality of timing violations based upon various input criteria.

13. The apparatus for optimizing buffers in an integrated circuit design of claim 12 wherein
the various input criteria include a median approach, the median approach including calculating a nominal number of fixes from the calculating possible solutions and then selecting an approach which fixes more than the nominal number of fixes.

14. The apparatus for optimizing buffers in an integrated circuit design of claim 12 wherein

the various input criteria include an acquisitive approach, the acquisitive approach including determining which solution from the calculating possible solutions fixes a greatest number of timing violations and then selecting the approach which fixes the greatest number of timing violations.

15. The apparatus for optimizing buffers in an integrated circuit design of claim 9 further comprising:

means for identifying buffers from a list of potential buffers available to insert into the integrated circuit design; and

means for choosing a subset of the buffers from the list as buffers for inserting at the particular nodes of the integrated circuit.

16. The apparatus for optimizing buffers in an integrated circuit design of claim 15 wherein:

factors used in choosing a subset of the buffers from the list as buffers include a first order delay characteristic of the buffer, a maximum time slack characteristic of the buffer, and a drive strength characteristic of the buffer.

17. A system for optimizing buffers in an integrated circuit design comprising:

an identifying module, the identifying module identifying paths and nodes within the integrated circuit design;

a determining module, the determining module determining node overlap within the integrated circuit design;

a calculating module, the calculating module calculating possible solutions for addressing timing violations within the integrated circuit design;

a choosing module, the choosing module choosing a solution for addressing timing violations;

an inserting module, the inserting module inserting buffers at particular nodes of the integrated circuit design; and,

a repeating module, the repeating module repeating the calculating possible solutions, the choosing a solution and the inserting buffers at particular nodes to address timing violations within the integrated circuit design.

18. The system for optimizing buffers in an integrated circuit design of claim 17 wherein

the repeating continues until a previous maximum number of violations have been addressed.

19. The system for optimizing buffers in an integrated circuit design of claim 18 wherein

after the repeating, there are orphan timing violations remaining to be addressed; and, further comprising

an orphan inserting module, the orphan inserting module inserting buffers at particular locations to address the orphan timing violations.

20. The system for optimizing buffers in an integrated circuit design of claim 18 wherein

the choosing a solution is based upon fixing a plurality of timing violations based upon various input criteria.

21. The system for optimizing buffers in an integrated circuit design of claim 20 wherein

the various input criteria include a median approach, the median approach including calculating a nominal number of fixes from the calculating possible solutions and then selecting an approach which fixes more than the nominal number of fixes.

22. The system for optimizing buffers in an integrated circuit design of claim 20 wherein

the various input criteria include an acquisitive approach, the acquisitive approach including determining which solution from the calculating possible solutions fixes a greatest number of timing violations and then selecting the approach which fixes the greatest number of timing violations.

23. The system for optimizing buffers in an integrated circuit design of claim 9 further comprising:

an identifying module, the identifying module identifying buffers from a list of potential buffers available to insert into the integrated circuit design; and

a subset choosing module, the subset choosing module choosing a subset of the buffers from the list as buffers for inserting at the particular nodes of the integrated circuit.

24. The system for optimizing buffers in an integrated circuit design of claim 23 wherein:

factors used in choosing a subset of the buffers from the list as buffers include a first order delay characteristic of the buffer, a maximum time slack characteristic of the buffer, and a drive strength characteristic of the buffer.